SESSION 23 – Honolulu Suite
Flash Memory II

Thursday, June 17, 3:25 p.m.
Chairpersons: D. Shum, Infineon
W-S Lee, Samsung Electronics

23.1 — 3:25 p.m.
A 70nm NOR Flash Technology with 0.049 μm^2 Cell Size, C. Park, S. Sim, J. Han, C. Jeong, Y. Jang, J. Park, J. Kim, K. Park and K. Kim, Samsung Electronics Co., Ltd., Gyunggi-Do, Korea

For first time, a 70nm NOR flash technology has been developed with a cell size of 0.049um2, which is the smallest size of NOR flash cell. The successful operation of 120nm-gate-length cell is achieved with three key technologies; an optimized Self-Aligned Poly (SAP) structure with top corner rounding trench structure, a small contact process with ArF photo lithographic tool, and a cell transistor engineering for the gate length of 120nm.

23.2 — 3:50 p.m.
Full Integration and Characterization of Localized ONO Memory (LONOM) for Embedded Flash Technology, I.W. Cho, B.R. Lim, J.-H. Kim, S.S. Kim, K.C. Kim, B.J. Lee. G.J. Bae, N.I. Lee, S.H. Kim, K.W. Koh. H.-K. Kang, M.K. Seo, S.W. Kim, S.H. Hwang, D.Y. Lee, M.C. Kim, S.D. Chae, S.A. Seo and C.W. Kim, Samsung, Kyunggi-Do, Korea

We have successfully integrated 8M bits Localized ONO Memory (LONOM) for the embedded nonvolatile memory using 0.13um standard logic process with 5-level Cu metallization, which has a small cell size of 0.276um2 and the simplest cell array structure. Without any special algorithm, the localized storage layer of the LONOM can satisfy the essential features for an embedded memory solution, such as low program current, disturb-free read operation and good endurance characteristics. The read speed is as high as 60MHz at Vcc=0.9V, 85 C and the current consumption is lower than 5mA at Vcc=1.4V.

23.3 — 4:15 p.m.
Charge-injection Length in Silicon Nanocrystal Memory Cells, T. Osabe, T. Ishii, T. Mine, T. Sano*, T. Arigane, T. Fukumura**, H. Kurata, S. Saeki*, Y. Ikeda** and K. Yano, Hitachi, Ltd., Tokyo, Japan, *Renesas Northern Japan Semiconductor, Inc., Tokyo, Japan, **Renesas Technology Corp., Hyogo, Japan

We present the first experimental investigation of the lateral charge-injection length for silicon nanocrystal memory cells programmed with source-side injection (SSI). Charge-pumping measurements reveal that the injection length of SSI programming is reducible to 24 nm and suggest the possibility of scaling down the nanocrystal memory for 2-bit/cell operation to the 90-65-nm range of technology nodes.

23.4 — 4:40 p.m.
Sub 40nm Tri-Gate Charge Trapping Nonvolatile Memory Cells for High Density Applications, M. Specht, R. Kömmling, L. Dreeskornfeld, W. Weber, F. Hofmann, D. Alvarez , J. Kretz, R.J. Luyken, W. Röesner, H. Reisinger*, E. Landgraf, T. Schulz, J. Hartwich, M. Städele, V. Klandievski, E. Hartmann**, L. Risch, Infineon Technologies AG, Munich, Germany, *MP INN, Munich, Germany, **SOPRA GmbH, Munich, Germany

Fully-depleted tri-gate oxide-nitride-oxide transistor memory cells with very short gate lengths in the range LG = 30 - 80 nm have been fabricated for the first time. The devices show excellent electrical characteristics and have been optimized successfully for high density NAND nonvolatile memory applications.